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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
ENGLUND, TERRY LEE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/761,239	CHOI, JONG-HYUN	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,10-13,16-24,26,29-33 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,10-13,16-18,29-33 and 35-37* is/are rejected.

7)☒ Claim(s) *19-24 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Oct 25, 2007 was reviewed and considered with the following results:

The comments with respect to the rejections of claims 10-13 and 15-18 under 35 U.S.C. 112 were not persuasive and those rejections have been maintained. These rejections are described later under the appropriate section, and associated comments are described under the Response to Arguments section.

The cancellation of claims 5 and 15 rendered their rejections moot.

The cancellation of claim 28 rendered its objection moot, but the addition of claim 28's allowable material into claim 19 created new objections and rejections. These are described later under the appropriate sections.

The amended claims overcame all of the prior art rejections described in the previous Office Action. Therefore, the following rejections have been withdrawn: 1) claims 1-3, 6, 10-13, 16-18, 32-33, and 35-37 under 35 U.S.C. 103(a), with respect to Hardee/Amanai; and 2) claims 1-3, 6, 10-13, 16, 19-24, 26, 32-33, and 35-37 under 35 U.S.C. 103(a), with respect to Wright et al./Amanai. None of these references clearly shows or discloses an inverter coupled to the connection node of the first and: 1) the third MOS transistors as now cited within claim 1; or 2) the second transistor as now cited within claim 10. Also, neither reference clearly shows or discloses the first internal node coupled to a row decoder and driver block as now cited within claim 19. Although those previous claim rejections have now been withdrawn, some of the

claims are now rejected using the same references, with some modifications taking into account the amended changes. These rejections are described later under the appropriate section.

When reviewing all of the active claims, various objections, and rejections under 35 U.S.C. 112, were noted. These are also described later under the appropriate section.

Claim Objections

Claims 19-24, 26, 32-33, and 35-37 are objected to because of the following informalities: Claim 19, line 5 "the memory" should be --a memory--, and line 7 "the row" should be --a row--, since these are the first time the memory device and row address signal are identified within the claim. However, related to these changes, "a row" and "a memory" cited on lines 15-16 of claim 19 should be changed to --the row-- and --the memory--to correspond to the newly added row address signal and memory device limitations now cited within amended lines 5 and 7. It is suggested --and-- be added after "voltage;" on line 6 of claim 32 to more clearly identify the last main limitation (i.e. "an interface circuit") is being identified within the claim. Since "the drain" of the second MOS transistor has not been previously identified, it is also suggested "the drain" on line 3 of claim 36 be changed to --a drain--. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-13 and 16-18 remain rejected, and claims 29-31 are now rejected, under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not

understood why the drain/source limitations of all the transistors within claim 10 were changed in a previous amendment. Although the drain/source connections of the first transistor do correspond to the applicant's figures, the drain/source connections of the second and third transistors are considered reversed with respect to what one of ordinary skill in the art would understand, and are therefore misleading. For example, which of the applicant's figures actually shows the source of the second transistor coupled to the output terminal, while the drain of the third transistor is coupled to a ground voltage? Using the applicant's own Fig. 1 as an example, isn't the drain of second transistor MN1 coupled to output terminal OUT, and the source of third transistor MN2 coupled to ground VSS? Claims 29-31 now depend on cancelled claim 28. Dependent claims carry over any rejection(s) from an claim(s) they depend upon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 10-13, 16-18, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee, in view of Amanai, wherein both references were cited in the previous Office Action. One of ordinary skill in the art would understand that Fig. 1 of Hardee shows a level shifting type device for receiving an input signal alternating between 0V and VCC, and for effectively providing a corresponding output signal that will selectively alternate between

0V and VCCP. The device comprises first internal circuit 12, including first MOS transistor 12, operating at first voltage VCCP higher than power supply voltage VCC of the device (e.g. see column 1, lines 25-28); second internal circuit 16, including second MOS transistor 16, operating at second voltage VCC lower than first voltage VCCP; and restricting means 14, including third MOS transistor 14 with a thin gate insulation layer (i.e. THIN OXIDE) and operating at second voltage VCC, wherein restricting means 14 will restrict a voltage transmitted from first internal circuit 12 to second internal circuit 16 by applying the voltage from first internal circuit 12 to second internal circuit 16 through third MOS transistor 14. Although second MOS transistor 16 is controlled by the input signal alternating between VCC and 0V, this signal is neither clearly shown nor disclosed as being related to a row address signal in a memory device. However, one of ordinary skill in the art would understand Hardee's device would be capable of operating with a row address signal as its input signal. Column 1, lines 24-28 of Hardee disclose the device relates to memory devices which may require the higher voltage, and therefore could be used with a memory device and its related signals. Amanai shows and discloses a memory related device utilizing a row address signal and a level shifter. For example, Fig. 1 of Amanai shows level shifter 15 controlled by a row address signal provided through gate 13. Therefore, it would have been obvious to one of ordinary skill in the art to supply second MOS transistor 16 of Hardee with a row address signal in a memory device, and/or to replace Amanai's cross coupled level shifting type circuitry 15 with two of Hardee's level shifting devices (two are required to respond to, and provide, complementary type signals to correspond to Amanai's complementary inputs and outputs), wherein Hardee's second MOS transistor 16 would be controlled by at least one row address signal through Amanai's logic gate 13. [Note: Hardee's transistor 16 would

receive the row address signal since it is the transistor receiving the alternating input signal. Transistor 14 receives VCC as its bias voltage.] It also would have been obvious to one of ordinary skill in the art to couple an inverter to an output connection node between the first and third MOS transistors (i.e. 12 and 14, respectively) of Hardee, wherein the inverter would drive a word line in the memory device, rendering claim 1 obvious. The inverter would provide an inverted version of the output signal from Hardee's circuit, if it was desired or required, and also provide one means for isolating the word line from Hardee's device. The type of signal applied to Hardee's second MOS transistor would depend on what type of input signal is to be shifted to provide a higher "high" level output. Since first MOS transistor 12 has a thick gate insulation layer (i.e. THICK OXIDE), and second MOS transistor 16 has a thin gate insulation layer (i.e. THIN OXIDE), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 12 to second internal circuit 16 would reduce an electric field applied to the gate insulation layer of second MOS transistor 16 since restricting means 14 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCC is a power supply voltage that would be either an external power supply voltage, or an internal power supply voltage, for the device, and claim 3 is rendered obvious. It would be obvious to one of ordinary skill in the art that the inverter include PMOS and NMOS transistors operating at a third voltage VCCP (of Hardee) higher than power supply voltage VCC, wherein each transistor would have a thick gate insulation layer. This renders claim 6 obvious. The inverter would include PMOS and NMOS transistors to closely correspond to the MOS transistors in Hardee's device, thus allowing all the transistors to have similar fabrication processes and operating characteristics. The inverter transistors will have a thick oxide to

prevent their breakdown, since they operate at the higher voltage VCCP. Interpreting Hardee's Fig. 1 circuit in a slightly different manner, the device comprises an output terminal (i.e. the unlabeled connection between transistors 12 and 14) selectively receiving high voltage VCCP higher than power supply voltage VCC of the device; first transistor 12 having a drain coupled to the output terminal, a source coupled to high voltage VCCP, a gate coupled to a first input signal that selectively alternates between 0V and VCCP, and a thick gate insulation layer (i.e. THICK OXIDE); second transistor 14 having a drain coupled to the output terminal, a gate coupled to low voltage VCC lower than high voltage VCCP, and a thin gate insulation layer (i.e. THIN OXIDE); and third transistor 16 having a drain coupled to the source of second transistor 14, a source coupled to a ground voltage, a gate coupled to a second input signal selectively alternating between 0V and VCC, and a thin gate insulation layer (i.e. THIN OXIDE). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 16 is capable of being, or with respect to Amanai can be, a row address signal from a memory device, and an inverter for driving a word line of a memory could obviously be coupled to a connection node of the first and second transistors as now cited within claim 10. Therefore, claim 10 is rendered obvious. Since second voltage VCC is the power supply voltage, which is an external power supply voltage, or an internal power supply voltage, of the device, claim 11 is also rendered obvious. One of ordinary skill in the art would understand that 0V is a low level corresponding to the ground voltage. Therefore, the first input signal is selectable as one of a high level of high voltage VCCP and a low level of ground; and the second input signal is selectable as one of a high level of low voltage VCC and a low level of ground, rendering claims 12-13 obvious. Claim 16 is rendered obvious for the same reasoning as

previously described above with claim 6. Hardee discloses that any number of NMOS transistors can be coupled in series to configure the switching circuit into a NAND logic configuration (e.g. see column 4, lines 29-36 and Fig. 4B). Therefore, it would have been obvious to one of ordinary skill in the art to couple a fourth transistor between third transistor 16 of Hardee and ground. This fourth transistor would have a thin gate insulation layer because it is related to the lower voltages within the device, not high voltage VCCP. Therefore, claim 17 is rendered obvious. The fourth transistor would provide another means for dropping voltage, thus helping to distribute the total voltage drop between the output terminal and ground across more transistors. Also, if the fourth transistor is used as part of a NAND logic configuration, it is capable of receiving a block selecting signal from the memory device, rendering obvious claim 18. Configured as NAND logic, the device will provide a low output signal only when the second input signal, and the block selecting signal, allow the third and fourth transistors to conduct. This will help ensure that the device will generate a low only when these specific conditions are met, and only when a low output signal is actually desired. By re-identifying the restricting means of claim 1 as an interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 14 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VCCP from being directly applied to the drain of second MOS transistor 16, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 16 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 16. This knowledge renders respective claims 36 and 37 obvious.

Claims 1-3, 6, 10-13, 16, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being Wright et al. (Wright), in view of Amanai, wherein both references have been previously cited (e.g. in the previous Office Action). Wright shows a semiconductor integrated circuit device in Fig. 2 comprising level shifter 200 comprising six MOS transistors 202-212 and inverter 214. This basic structure corresponds to transistors MN11-MN12, MN9-MN10, and MP5-MP6 and inverter INV2, respectively shown in the applicant's Fig. 4. Therefore, one of ordinary skill in the art would understand Wright's configuration has a device comprising first internal circuit 212, including first MOS transistor 212, operating at first voltage VIO higher than power supply voltage VCORE of the device (e.g. see column 1, lines 28-32 and 48-50); second internal circuit 204, including second MOS transistor 204, operating at second voltage VCORE (i.e. inverted VIN, on line 224, will have VCORE as its high logic level) lower than first voltage VIO; and restricting means 208, including third MOS transistor 208 that can have a relatively thin gate insulation layer (e.g. see column 4, line 17-19, wherein a medium gate oxide is relatively thinner than a thick gate oxide) and operating at second voltage VCORE, wherein one of ordinary skill in the art will know restricting means 208 will restrict a voltage transmitted from first internal circuit 212 to second internal circuit 204 by applying the voltage from first internal circuit 212 to second internal circuit 204 through third MOS transistor 208. Second MOS transistor 204 is controlled by the inverted input signal VIN. However, VIN is neither clearly shown nor disclosed as a row address signal. Fig. 1 of Amanai shows level shifter 15 that corresponds to Wright's Fig. 1, wherein Wright modified Fig. 1 to obtain the level shifter shown in Wright's Fig. 2. Amanai's level shifter 15 is controlled with respect to a row address signal supplied through logic gate 13, and it would have been obvious to one of ordinary skill in the art to

effectively supply a row address signal as VIN to Wright's circuit. It also would have been obvious to connect node 220 of Wright, between first/third MOS transistors 212/208 to an inverter that drives a WL of the memory device, rendering claim 1 obvious. The inverter would allow isolation between the level shifter and subsequent circuitry, and provide an inverted signal at the proper levels when necessary. For example, the use of Wright's circuit in a memory, for level shifting a row address signal, is one type of intended use one of ordinary skill in the art would understand. Since first MOS transistor 212 has a thick gate insulation layer (i.e. see column 4, lines 17-18), and second MOS transistor 204 has a relatively thin gate insulation layer (i.e. see column 4, line 4), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 212 to second internal circuit 204 would reduce an electric field applied to the gate insulation layer of second MOS transistor 204 since restricting means 208 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCORE is a power supply voltage that is an internal power supply voltage for the device (e.g. see column 1, line 48-50), and claim 3 is rendered obvious. The inverter would obviously include PMOS/NMOS transistors operating at a third voltage VIO higher than power supply voltage VCORE when transistor 212 is conducting, wherein each transistor of the inverter would have a thick gate insulation layer because of the higher voltage. This renders claim 6 obvious. The MOS transistors would allow the inverter to operate under the same operating characteristics of the MOS transistors within Wright's circuit. Also, when all of the transistors within a circuit are made from the same basic types of transistors (e.g. MOS or bipolar), circuit fabrication is easier. Interpreting the Wright/Amanai configuration in a slightly different manner, the device comprises output terminal 220 selectively receiving high voltage

VIO higher than power supply voltage VCORE; first transistor 212 having a drain coupled to output terminal VOUT, a source coupled to high voltage VIO, a gate coupled to a first input signal (from the common connection between 210 and 206), and a thick gate insulation layer (i.e. thick gate oxide); second transistor 208 having a drain coupled to output terminal VOUT, a gate coupled to low voltage VCORE lower than high voltage VIO, and a relatively thin gate insulation layer (i.e. a medium gate oxide is thinner than a thick gate oxide); and third transistor 204 having a drain coupled to the source of second transistor 208, a source coupled to a ground voltage, a gate coupled to a second input signal (i.e. an inverted version of Wright's input signal VIN, which corresponds to the row address signal supplied via Amanai's logic gate 13 as previously described), and a thin gate insulation layer (i.e. thin gate oxide). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 204 effectively includes a row address signal from a memory device, and an inverter for driving a word line could be coupled to a connection node of the first and second transistors as now cited within claim 10. Therefore, claim 10 is rendered obvious. Since second voltage VCORE is the power supply voltage that is an internal power supply voltage of the device, claim 11 is also rendered obvious. The first input signal, generated at the common connection between 210 and 206, is selectable as one of a high level of high voltage VIO when transistor 210 is conducting, and a low level of ground when transistor 202 is conducting, thus rendering claim 12 obvious. The second input signal, provided at the output of Wright's inverter 214, is selectable as one of a high level of low voltage VCORE and a low level of ground, rendering claim 13 obvious. Claim 16 is rendered obvious for the same reasoning as previously described with respect to claim 6.By re-identifying the restricting means of claim 1 as an

interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 208 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VIO from being directly applied to the drain of second MOS transistor 204, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 204 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 204. This knowledge renders respective claims 36 and 37 obvious.

No claim is allowable as presently written.

Claims 4-5, 7-9, 14-15, 25, 27-28, and 34 have been cancelled.

Allowable Subject Matter

Claims 19-24, and 26 are now only objected to for the reasons described above. However, they would be allowable if independent claim 19 is satisfactorily rewritten to overcome its objections. There is presently no motivation to modify or combine any prior art reference(s) to ensure the first internal node is coupled to a row decoder and driver block of the memory device, wherein that block selectively drives word lines of the memory device in response to a row address signal, as now recited within claim 19, upon which claims 20-24 and 26 depend.

Also, claims 29-31 would be allowable if rewritten to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. It is believed these claims were meant to depend on claim 19, which was only objected to as described above.

Response to Arguments

The applicant's arguments filed Oct 25, 2007 have been fully considered but they are not persuasive with respect to claim 10. The drain and source of an NMOS transistor are typically connected to higher and lower voltages respectively. For example, when an NMOS transistor is coupled to ground, the source is the terminal coupled to ground, wherein the drain is coupled to a voltage higher than ground. However, if a PMOS transistor is coupled to ground, it has its drain coupled to ground. Therefore, the source and drain connections of the second and third transistors within claim 10 are considered reversed with respect to what is actually shown within the applicant's figures. Otherwise, the applicant is requested to identify which particular figure clearly shows a third transistor having its drain coupled to ground as cited on lines 10-11 of claim 10. The applicant comments that it is presumed the examiner meant transistor 14 of Hardee receives the row address signal instead of transistor 16. However, the examiner disagrees. Hardee's transistor 16 is clearly shown receiving an alternating input signal, while transistor 14 receives VCC as its bias voltage. Therefore, it would be obvious to one of ordinary skill in the art that the transistor receiving the alternating input signal would be capable of receiving a row address signal as that alternating input signal. The applicant also argues that it wouldn't make sense to combine the two different types of level shift circuits of Hardee and Amanai. Although one of ordinary skill in the art would understand one level shift circuit can be replaced with another functionally equivalent circuit, the claim rejections have been modified to more clearly indicate the obvious type modifications meant since the examiner did not intend to imply that a single transistor of Hardee is replaced with the cross-coupled transistors of Amanai. The applicant also argues that if the subject matter of claim 28 is allowable, amended claims 1

and 10 are also allowable. However, it is noted that cancelled claim 28 had cited a row decoder and a driver block as being coupled to the first internal node. If the applicants are implying that the single inverter (a driver) now cited within claims 1 and 10 is the same as "a row decoder and a driver block", then the examiner will have to reject at least claim 19 (which now includes the claimed limitations of cancelled claim 28) in the next Office Action. It is not understood why one of ordinary skill in the art would not considered Wright's level shifting circuitry and Amanai's level shifting circuitry are not compatible. For example, the level shifter shown in Wright's Fig. 1 corresponds to Amanai's level shifter, wherein Wright's Fig. 2 is a modified version of Fig. 1 having an extra pair of transistors (206 and 208) inserted between the original pairs of PMOS and NMOS transistors. Therefore, what prevents the level shifter of Wright from receiving a row address signal at VIN, and what prevents the use of Wright's level shifter as the level shifter's used within Amanai's overall circuit? One of ordinary skill in the art would find these references are compatible, and obvious modifications can be made between the teachings and circuitry shown/disclosed within both of them.

Therefore, the rejections described in this Office Action are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations, and what is shown, disclosed, and known in the prior art.

Prior Art

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed limitations. Fig. 10 of Lee shows the use inverter 126 (or 127) for driving word line RMWLb<i>, wherein the inverter is coupled to a connection of transistors P5 and N30 of a level shifter type circuit. Choi et al. shows an example of using inverter 435

coupled to a connection of two series transistors within a level shifter comprising cross-coupled sets of transistors. Therefore, these references should be reviewed and considered with respect to the broadest reasonable interpretation of the claimed limitations, and of what is shown and disclosed by prior art references.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Drew Richards, can be reached on (571) 272-1736.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

19 January 2008

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER